PROCESS FOR OPTIMIZING JUNCTIONS FORMED BY SOLID PHASE
EPITAXY

TECHNICAL FIELD OF THE INVENTION

This invention relates generally to the field of semiconductor devices and, more particularly, to a method for optimizing junctions formed by solid phase epitaxy.

BACKGROUND

As semiconductor manufacturers continue to reduce the scale of semiconductor devices, the junction depth associated with the junction areas likewise tends to

5   decrease. Conventional methods for activating a majority of the dopants within the junction areas of the semiconductor device typically require a high temperature anneal, which often leads to increased dopant diffusion from the junction areas. Methods to reduce the junction

10 depth often result in an increase in semiconductor device sheet resistance and a lower semiconductor device drive current.

SUMMARY

In one method embodiment, a method of forming a semiconductor device comprises forming at least one amorphous region within an at least partially formed

5   semiconductor device. The method also comprises implanting a halogen species in the at least one amorphous region of the at least partially formed semiconductor device. The method further comprises doping at least a portion of the at least one amorphous

10 region to form at least one junction within the at least partially formed semiconductor device. The method also comprises activating the doped portion of the at least one amorphous region of the at least partially formed semiconductor device by solid phase epitaxial re-growth.

15 In one embodiment, a transistor is formed using a method. The method comprises implanting at least a halogen species within an at least partially formed semiconductor device to form at least one amorphous region. The method also comprises doping at least a

20 portion of the at least one amorphous region to form at least one junction within the at least partially formed semiconductor device. The method further comprises activating the doped portion of the at least one amorphous region of the at least partially formed

25 semiconductor device by solid phase epitaxial re-growth.

Depending on the specific features implemented, particular embodiments of the present invention may exhibit some, none, or all of the following technical advantages. Various embodiments minimize leakage current

30 from the junction areas of the semiconductor device after solid phase epitaxial re-growth. Some embodiments may increase the gradient of boron concentration after solid phase epitaxial re-growth.

Other technical advantages will be readily apparent to one skilled in the art from the following figures, descriptions and claims. Moreover, while specific advantages have been enumerated above, various embodiments may include all, some or none of the enumerated advantages.

BRIEF DESCRIPTION OF THE DRAWINGS

For a more complete understanding of the present invention, and for further features and advantages thereof, reference is now made to the following

5   description taken in conjunction with the accompanying drawings, in which:

FIGURES 1A through 1F are cross sectional views illustrating one example of a method of forming a portion of a semiconductor device; and

10   FIGURE 2 is a graph comparing the boron diffusion during solid phase epitaxial re-growth of a semiconductor device with a fluorine-based amorphous region to a semiconductor device without a fluorine-based amorphous region.

DETAILED DESCRIPTION OF EXAMPLE EMBODIMENTS

FIGURES 1A through 1F are cross-sectional views showing one example of a method of forming a portion of semiconductor device 10. Semiconductor device 10 may be

5   used as a basis for forming any of a variety of semi-conductor devices, such as a bipolar junction transistor, a NMOS transistor, a PMOS transistor, a CMOS transistor, or other semiconductor based devices. Particular examples and dimensions specified throughout

10   this document are intended for example purposes only, and are not intended to limit the scope of the present disclosure. Moreover, the illustration in FIGURES 1A through 1F are not intended to be to scale.

One aspect of this disclosure recognizes that

15   implanting a halogen species in an amorphous region (to be formed later) of semiconductor device 10 can minimize lattice defects in the amorphous region. Implanting a halogen species in the amorphous region of semiconductor device 10 can alleviate some of the problems

20   conventionally associated with the lattice defects in the amorphous regions of the semiconductor device.

FIGURE 1A shows a cross sectional view of semiconductor device 10 after formation of a gate dielectric layer 13 disposed outwardly from a

25   semiconductor substrate 12 and after formation of a gate electrode layer 14 outwardly from gate dielectric layer 13. Although gate dielectric layer 13 and gate electrode layer 14 are shown as being formed without interstitial layers between them, such interstitial layers could

30   alternatively be formed without departing from the scope of the present disclosure. Semiconductor substrate 12 may comprise any suitable material used in semiconductor chip fabrication, such as silicon or germanium. Gate

dielectric layer 13 may comprise, for example, oxide, silicon dioxide, or oxi-nitride.

Forming gate dielectric layer 13 may be effected through any of a variety of processes. In one non-limiting example, gate dielectric layer 13 can be formed by growing an oxide. Using a grown oxide as gate dielectric layer 13 is advantageous in providing a mechanism for removing surface irregularities in semiconductor substrate 12. For example, as oxide is grown on the surface of substrate 12, a portion of substrate 12 is consumed, including at least some of the surface irregularities.

At some point, the active areas of semiconductor device 10 can be formed. Active areas of semiconductor device 10 may be formed, for example, by doping those areas to adjust the threshold voltage V_t of semiconductor device 10. This doping may comprise, for example, ion implantation through gate dielectric layer 13. In an alternative embodiment, doping of the active regions of semiconductor device 10 can occur before formation of gate dielectric layer 13. In one particular embodiment (not explicitly shown), a sacrificial dielectric layer may be disposed before formation of gate dielectric layer 13. In that case, the active regions of semiconductor device 10 are doped by implantation through the sacrificial dielectric layer. Then, the sacrificial dielectric layer is removed, and gate dielectric layer 13 is formed.

Gate electrode layer 14 may comprise, for example, amorphous silicon or polysilicon. In this example, gate electrode layer 14 comprises polysilicon. Forming gate electrode layer 14 may be effected, for example, by depositing polysilicon.

In some embodiments, after forming gate electrode layer 14, gate electrode layer 14 may be doped to achieve a desired gate to junction capacitance. Gate electrode layer 14 may be doped through any of a variety of

5   processes, such as, for example, by ion implantation. In various embodiments, ion implantation of gate dielectric layer 14 may comprise, for example, a boron dopant, a phosphorous dopant, and/or an arsenic dopant.

FIGURE 1B shows a cross sectional view of

10   semiconductor device 10 after formation of a semiconductor gate 16 outwardly from substrate 12. Forming semiconductor gate 16 may be effected through any of a variety of processes. For example, semiconductor gate 16 can be formed by patterning and etching gate

15   electrode layer 14 and gate dielectric layer 13 using photo resist mask and etch techniques.

FIGURE 1C shows a cross sectional view of semiconductor device 10 after formation of a first screen dielectric layer 18 outwardly from semiconductor

20   substrate 12 and after formation of a first spacer layer 20 outwardly from first screen dielectric layer 18. Although first screen dielectric layer 18 and first spacer layer 20 are shown as being formed without interstitial layers between them, such interstitial could

25   alternatively be formed without departing from the scope of the present disclosure. First screen dielectric layer 18 may comprise, for example, silicon oxide or silicon oxi-nitride.

Forming first screen dielectric layer 18 may be

30   effected through any of a variety of processes. For example, first screen dielectric layer 18 can be formed by growing an oxide. In this particular embodiment, first screen dielectric layer 18 combines with gate dielectric layer 13 during the formation of layer 18.

Using a grown oxide as first screen dielectric layer 18 is advantageous in providing a mechanism for removing surface irregularities in substrate 12 and semiconductor gate 16 created during the formation of gate 16.

5   First spacer layer 20 may comprise any dielectric material, such as, for example, silicon nitride, silicon oxi-nitride, or silicon oxide. Forming first spacer layer 20 may be effected through any of a variety of processes. In one non-limiting example, first spacer

10   layer 20 can be formed by depositing a silicon nitride.

In the illustrated embodiment, first screen dielectric layer 18 comprises a dielectric material that is selectively etchable from first spacer layer 20. That is, each of first screen dielectric layer 18 and first

15   spacer layer 20 can be removed using an etchant that does not significantly affect the other. In one non-limiting example, first screen dielectric layer 18 may comprise a layer of silicon oxide while first spacer layer 20 may comprise silicon nitride. In an alternative embodiment,

20   first spacer layer 20 can comprise a dielectric material that is incapable of being selectively etched from first screen dielectric layer 18.

In this particular embodiment, first spacer layer 20 is formed outwardly from first screen dielectric layer

25   18. In an alternative embodiment, the thickness of first screen dielectric 18 may be increased to a point that substantially negates the need for the formation of first spacer layer 20 outwardly from first screen dielectric layer 18. In this example, the formation of first screen

30   dielectric layer 18 may be effected, for example, by growing a silicon oxide, by depositing a silicon oxide, or a combination of growing and depositing a silicon oxide.

FIGURE 1D shows a cross sectional view of semiconductor device 10 after removal of at least a portion of first screen dielectric layer 18 and at least a portion of first spacer layer 20, and after formation of amorphous regions 22. Portions of first screen dielectric layer 18 and first spacer layer 20 may be removed, for example, by anisotropically etching first screen dielectric layer 18 and first spacer layer 20. In one non-limiting example, portions of first screen dielectric layer 18 and first spacer layer 20 are removed by performing a plasma etch.

In this embodiment, portions of first screen dielectric layer 18 disposed outwardly from amorphous regions 22 are completely removed. In an alternative embodiment, portions of first screen dielectric layer 18 remain disposed outwardly from amorphous regions 22 after removal of portions of layers 18 and 20. Leaving at least a portion of first screen dielectric layer 18 disposed outwardly from amorphous regions 22 can be advantageous in reducing surface irregularities of substrate 12 formed during the etching process.

Amorphous regions 22 of semiconductor device 10 can be formed by any of a variety of processes. In one non-limiting example, amorphous regions 22 of semiconductor device 10 can be formed by ion implantation. In various embodiments, amorphous regions 22 can be formed by implanting a dopant species capable of changing the phase of at least a portion of substrate 12 from a crystalline phase to an amorphous phase. The species implanted to form amorphous regions 22 may comprise, for example, a silicon species, a germanium species, and/or a halogen species. The dose and implantation energy utilized to form amorphous regions 22 depends at least in part on a desired amorphous region depth (X_α) and the dopant

species used to form amorphous regions 22. The amorphous region depth (X_α) depends at least in part on a desired junction depth (X_j) of device 10.

5   At some point, amorphous regions 22 of semiconductor device 10 can be formed. In various embodiments, amorphous regions 22 can be formed before forming screen dielectric layer 18 and first spacer layer 20. In some embodiments, amorphous regions 22 can be formed before removal of portions of first screen dielectric layer 18

10   and first spacer layer 20. In other embodiments, amorphous regions 22 may be formed after removal of at least a portion of first screen dielectric layer 18 and first spacer layer 20.

     One aspect of this disclosure recognizes that

15   implanting a halogen species in amorphous regions 22 can minimize lattice defects (e.g., dangling bonds and/or un-bonded orbitals) formed in amorphous regions 22 during ion implantation. Implanting a halogen species in amorphous regions 22 of semiconductor device 10 can

20   alleviate some of the problems conventionally associated with the lattice defects in the amorphous regions of the semiconductor device.

     Conventional methods of forming the amorphous regions in the substrate of the semiconductor device

25   often lead to lattice defects within the material used to form the semiconductor substrate. Lattice defects in the material can result in the formation of carrier generation-recombination centers in the space-charge region of the electrical junctions of the device after

30   solid phase epitaxial re-growth. The formation of these carrier generation recombination centers can result in the formation of leakage current within the device, which can degrade the semiconductor device performance.

Unlike conventional methods, semiconductor device 10 implants a halogen species within amorphous regions 22. Implanting a halogen species into amorphous regions 22 enables device manufacturers to reduce the formation of

5   carrier generation recombination centers in the space-charge region of the electrical junctions after solid phase epitaxial re-growth. The use of a halogen species in amorphous regions 22 provides the advantage of minimizing lattice defects in the space-charge region of

10   the electrical junctions after solid phase epitaxial re-growth. Minimizing lattice defects in the space-charge region of the electrical junctions is advantageous in minimizing leakage current from device 10.

In this particular embodiment, amorphous regions 22

15   are formed by implanting fluorine at an implantation dose of approximately 5×10^{14} cm^{-2} to 1×10^{16} cm^{-2} and an implantation energy of approximately 1 to 200 keV. In that case, the fluorine operates to minimize lattice defects in amorphous regions 22 by bonding to dangling

20   bonds, un-bonded orbitals, and/or any other lattice defect within the space-charge region of the electrical junctions.

In this example, the implantation of a fluorine species within semiconductor device 10 occurs during the

25   formation of amorphous regions 22. In an alternative embodiment, the implantation of a fluorine species can occur substantially simultaneously with or after the formation of amorphous regions 22. In that embodiment, amorphous regions 22 can be formed by implanting a

30   silicon species and/or a germanium species within semiconductor device 10. In that case, the formation of amorphous regions 22 can comprise implanting silicon and/or germanium at an implantation dose of approximately 1×10^{14} cm^{-2} to 1×10^{16} cm^{-2} and an implantation energy of

approximately 5 keV to 50 keV. In addition, the fluorine species can be implanted at an implantation dose of approximately 5×10^{13} cm^{-2} to 1×10^{16} cm^{-2} and an implantation energy of approximately 1 to 200 keV.

5   FIGURE 1E shows a cross sectional view of semiconductor device 10 after formation of junction areas 24 within amorphous regions 22. Junction areas 24 can comprise, for example, a source and a drain, or a source extension and a drain extension. In various embodiments, 10   junction areas 24 may comprise a relatively high-doping concentration of boron, phosphorous, and/or arsenic dopants. The dopant concentration of junction areas 24 depends at least in part on the desired sheet resistance of semiconductor device 10. Increasing the dopant 15   concentration in junction areas 24 typically results in a lower sheet resistance of semiconductor device 10.

        Junction areas 24 of semiconductor device 10 can be formed by any of a variety of processes. In one non-limiting example, junction areas 24 of semiconductor 20   device 10 can be formed by ion implantation. The dopant implanted to form junction areas 24 can comprise, for example, a boron dopant, a phosphorous dopant, an arsenic dopant, or a combination of these or other dopants. The dose and implantation energy utilized to form junction 25   areas 24 depends at least in part on a desired junction depth (X_j) and the dopant used to form junction areas 24. In this particular embodiment, junction areas 24 are formed by implanting boron at an implantation dose of approximately 1×10^{14} cm^{-2} to 4×10^{15} cm^{-2} and at an 30   implantation energy of approximately 200 eV to 2keV.

        The junction depth (X_j) of junction areas 24 depends at least in part on a gate length associated with semiconductor gate 16. Reducing the gate length of gate 16 typically results in shallower junction depths (X_j) of

junction areas 24.   In this example, junction areas 24 comprise a junction depth (X_j), after dopant activation, of three hundred (300) Angstroms or less.

At some point, junction areas 24 of semiconductor device 10 can be formed.   Junction areas 24 may be formed, for example, after formation of amorphous regions 22, and before removal of portions of first screen dielectric layer 18 and first spacer layer 20.   In another embodiment, extension areas 22 may be formed after formation of amorphous regions 22, and after removal of at least a portion of first screen dielectric layer 18 and first spacer layer 20.

In this example, the implantation of a fluorine species within semiconductor device 10 occurs during formation of amorphous regions 22.   In an alternative embodiment, the implantation of a fluorine species can occur after the formation of junction areas 24.   In that case, the fluorine species can be implanted at an implantation dose of approximately 5×10^{13} cm^{-2} to 1×10^{16} cm^{-2} and an implantation energy of approximately 1 to 200 keV.

One aspect of this disclosure recognizes that forming amorphous regions 22 with an amorphous depth (X_α) that is greater than or equal to the junction depth (X_j) can result in improved activation of the dopants in junction areas 24.   Forming an amorphous region depth (X_α) that is greater than or equal to the junction depth (X_j) can alleviate some of the problems conventionally associated with the activation of dopants in the junction areas of the semiconductor device.

Conventional methods for minimizing the impact of lattice defects of the material used to form the semiconductor substrate often lead junction depths (X_j)

that are greater than the amorphous region depth (X_α). A junction depth (X_j) that is greater than the amorphous region depth (X_α) typically results in reduced dopant activation during solid phase epitaxial re-growth.

5   Reducing dopant activation in the junction areas of the semiconductor device can result in an increase in semiconductor sheet resistance and a junction depth (X_j) that is not optimal.

Unlike the conventional methods, semiconductor

10 device 10 implements an amorphous depth (X_α) that is greater than or equal to the junction depth (X_j). Implementing an amorphous depth (X_α) that is greater than or equal to the junction depth (X_j) enables device manufacturers to optimize junction areas 24 by increasing

15 dopant activation in junction areas 24 during solid phase epitaxial re-growth. The optimization of dopant activation in junction areas 24 enables device manufacturers to obtain a lower sheet resistance, a desired drive current, and/or a relatively high gate to

20 junction capacitance.

Although increasing the amorphous region depth (X_α) can increase the number of lattice defects in the space-charge region of junction areas 24, device 10 counteracts this effect by implanting a halogen species into

25 amorphous regions 22. Implanting a halogen species into amorphous regions 22 tends to minimize the amount of lattice defects in the space-charge regions of junction areas 24 because the halogen species tends to bond to the lattice defects.

30 FIGURE 1F is a cross-sectional view of semiconductor device 10 after activation of the dopants in junction areas 24. The dopants of junction areas 24 can be activated by any of a number of processes, such as, for

example, by solid phase epitaxial re-growth. The solid
phase epitaxial re-growth process converts the amorphous
phase of the material in amorphous regions 22 to a
crystalline phase. In other words, solid phase epitaxial
5   re-growth re-crystallizes that portion of substrate 12
converted to an amorphous phase during implantation of
amorphous regions 22. This re-crystallization process
operates to activate the dopants within junction areas
24.

10   One aspect of this disclosure recognizes that
activation of a majority of the dopants within junction
areas 24 can occur at a relatively low temperature.
Activating a majority of the dopants within junction
areas 24 of semiconductor device 10 at a relatively low
15   temperature can alleviate some of the problems
conventionally associated with dopant diffusion during
relatively high temperature activation.

As semiconductor manufacturers continue to reduce
the scale of semiconductor devices, the junction depth
20   (X_j) associated with the junction areas likewise tends to
decrease. Conventional methods for activating a majority
of the dopants within the junction areas of the
semiconductor device typically require a relatively high
temperature anneal (e.g., 1000 to 1100 degrees Celsius).
25   Activating the dopants within the junction areas with a
relatively high temperature anneal often leads to
increased dopant diffusion, which can lead to junction
depths that are deeper than desired. To counteract this
effect, conventional methods often reduce the dopant
30   concentration within the junction areas and/or the
implantation energy of the dopants. Reducing the dopant
concentration of the junction areas typically results in
an increase in semiconductor device sheet resistance, a

lower semiconductor device drive current, and/or a reduced gate to junction capacitance.

Unlike conventional methods, dopant activation of junction areas 24 occurs in a relatively low temperature

5 environment. Activating the dopants in a relatively low temperature environment enables device manufacturers to minimize dopant diffusion from junction areas 24. Minimizing dopant diffusion from junction areas 24 advantageously allows device manufacturers to obtain a

10 relatively shallow junction depth (X_j) while obtaining a desired sheet resistance. In various embodiments, device manufacturers can obtain a junction depth of three hundred (300) Angstroms or less, and a sheet resistance of approximately five hundred (500) to one thousand

15 (1000) ohms/sq.

In this example, the amorphous depth (X_α) is greater than or equal to the junction depth (X_j). The amorphous phase of the material in amorphous regions 22 comprises a relatively higher energy state than the energy state of a

20 crystalline phase of the material. Consequently, activating the dopants within junction areas 24 by using solid phase epitaxial re-growth (e.g., converting the amorphous phase to a crystalline phase) advantageously enables device manufacturers to activate the dopants at a

25 relatively lower temperature. In this particular embodiment, the activation of the dopants in junction areas 24 comprises solid phase epitaxial re-growth at a temperature of approximately 500 to 700 degrees Celsius.

FIGURE 2 is a graph comparing the boron diffusion

30 during solid phase epitaxial re-growth of a semiconductor device with a fluorine-based amorphous region to a semiconductor device without a fluorine-based amorphous region. In this example, line 202 represents the diffusion of boron in the semiconductor device without

the fluorine-based amorphous region.   Line 204 represents
the diffusion of boron in the semiconductor device with
the fluorine-based amorphous region.   In this particular
example, the fluorine-based amorphous region is implanted

5   with fluorine at an implantation dose of approximately 1
$\times$ 10^{15} cm^{-2} and an implantation energy of approximately 12
keV.   The   horizontal   axis   represents   the   vertical
diffusion of the boron dopants, while the vertical axis
represents the concentration of the boron dopants in the

10   junction areas of each device.

In this example, each semiconductor device includes
an amorphous region formed by implanting germanium at an
implantation dose of approximately 5 $\times$ 10^{14} cm^{-2} and an
implantation   energy   of   approximately   48   keV.   Each

15   semiconductor   device   also   includes   a   junction   area
implanted with boron ions at an implantation dose of
approximately 1.2 $\times$ 10^{15} cm^{-2} and an implantation energy of
approximately   700   eV.   In   addition,   the   boron   ions
implanted in each semiconductor device are activated by

20   solid   phase   epitaxial   re-growth   at   a   temperature   of
approximately six hundred fifty (650) degrees Celsius for
approximately five (5) minutes.

This   graph   illustrates   that   implanting   a   fluorine
species within the amorphous region of a semiconductor

25   device can result in increased dopant diffusion from the
junction areas during solid phase epitaxial re-growth.
Device   manufacturers   can   control   the   dopant   diffusion
from the junction areas by varying the concentration of
the fluorine species.   Increasing the concentration of

30   fluorine   tends   to   increase   dopant   diffusion   from   the
junction areas.   In addition, varying the concentration
and implantation energy of the fluorine species can allow
device manufacturers to optimize the dopant concentration

profile within the junction areas. In other words, varying the concentration and implantation energy of fluorine can allow device manufacturers to balance the effects of fluorine on diffusion and the benefits of

5   fluorine in minimizing leakage current from the device. Similar results and benefits can be realized by implementing a halogen-based amorphous region.

Although the present invention has been described in several embodiments, a myriad of changes, variations,

10   alterations, transformations, and modifications may be suggested to one skilled in the art, and it is intended that the present invention encompass such changes, variations, alterations, transformations, and modifications as falling within the spirit and scope of

15   the appended claims.